Development of Heterogeneous Multiprocessing Digital Beam Position and Phase Monitor Electronics at HIAF-iLinac*

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The heavy-ion accelerator facility (HIAF) under construction in China will produce various stable and intense radioactive beams with energies ranging from MeV/u to GeV/u. The ion-linac (iLinac) accelerator, which will serve as the injector for the HIAF, is a superconducting heavy-ion accelerator containing 13 cryomodules. It will operate in either continuous wave mode or pulsed mode, with a beam current ranging from $0.01\,\mathrm{emA}$ to $1\,\mathrm{emA}$. The beam position monitor (BPM) is crucial for this high-beam-power machine, which requires precise beam control and a very small beam loss of less than $1\,\mathrm{W/m}$, especially inside the cryomodules of this unique beam instrument. Nearly 70 BPMs will be installed on the iLinac. New digital beam position and phase measurement (DBPPM) electronics based on a heterogeneous multiprocessing platform system-on-chip (MPSoC) has been developed to provide accurate beam trajectory and phase measurements as well as beam interlocking signals for a fast machine protection system (MPS). The DBPPM comprises an analog front-end (AFE) board in field programmable gate array (FPGA) mezzanine-connector (FMC) form factor, along with a digital signal processing board housed within a 2U 19" chassis. To mitigate radio frequency (RF) leakage effects from high-power RF systems in certain scenarios, beam signals undergo simultaneous processing at both fundamental and second-harmonic frequencies. A dynamic range from $-65\,\mathrm{dBm}$ to $0\,\mathrm{dBm}$ was established to accommodate both weak beam commissioning and high-intensity operational demands. Laboratory tests demonstrated that at input power levels exceeding $-45\,\mathrm{dBm}$, the phase resolution surpasses 0.05°, and the position resolution exceeds $5\,\mu\mathrm{m}$. These results align well with the stipulated measurement requirements. Moreover, the newly developed DBPPM has self-testing and self-calibration functions that are highly helpful for the systematic evaluation of numerous electronic components and fault diagnosis equipment. In addition, the DBPPM electronics implements a 2D non-linear polynomial correction on the FPGA and can collect accurate real-time position measurements at large beam offsets. This newly developed DBPPM electronics has been applied to several Linac machines, and the results from beam measurements show high performance, good long-term stability, and high reliability. In this paper, a detailed overview of the architecture, performance, and proof-of-principle measurement of the beams is presented.

Keywords: HIAF, beam position and phase monitor, digital signal processing, FPGA

I. INTRODUCTION

The heavy-ion accelerator facility (HIAF) [1–3] is a next-generation storage-ring-based heavy-ion research facility that focuses on interdisciplinary studies in nuclear physics, nuclear astrophysics, atomic physics, and heavy-ion applications. It was approved by the Chinese government in 2015, and its construction started in December 2018. The installation has begun, and the machine commission is scheduled for 2025. HIAF will be one of the world's leading heavy-ion accelerator complexes in the envisaged future, capable of producing various stable and radioactive intense beams with energies ranging from MeV/u to GeV/u. Figure 1 illustrates the layout of the HIAF facility. Ion beams ranging from protons to uranium are generated by a superconducting electron cyclotron resonance (SECR) ion source and accelerated by an ion-linac (iLinac) to $17\,\mathrm{MeV/u}$ for U^{35+} ions. These beams are then either transferred to the booster ring (BRing) synchrotron for accumulation and further acceleration, or directed to the low-energy nuclear structure terminal equipped with a nuclear structure spectrometer and low-energy irradiation target. When serving as the injector for the BRing, the iLinac requires a pulsed-mode operation with a pulse length ranging from $0.2\,\mathrm{ms}$ to $2\,\mathrm{ms}$ and a maximum repetition rate of $5\,\mathrm{Hz}$. During the BRing commissioning phase, the pulse length will be shortened to $1\,\mu\mathrm{s}$ to optimize the first few turns of the beam trajectory. By contrast, when the beam is routed to a low-energy nuclear structure terminal, a continuous-wave (CW) beam or a similar high-duty-ratio CW beam is required. To maximize the integrated beam time, beam splitting is executed at these two locations for certain beams, as shown in Figure 2. This indicates that the iLinac functions in a similar manner to a dedicated facility for various programs, analogous to the digital beam position and phase measurement (DBPPM) system.

At the iLinac, very-low-energy beams are accelerated by radio frequency quadrupole (RFQ) and quarter wave resonator (QWR) superconducting radio frequency (SRF) cavities operating at a frequency of $81.25\,\mathrm{MHz}$ and then by half-

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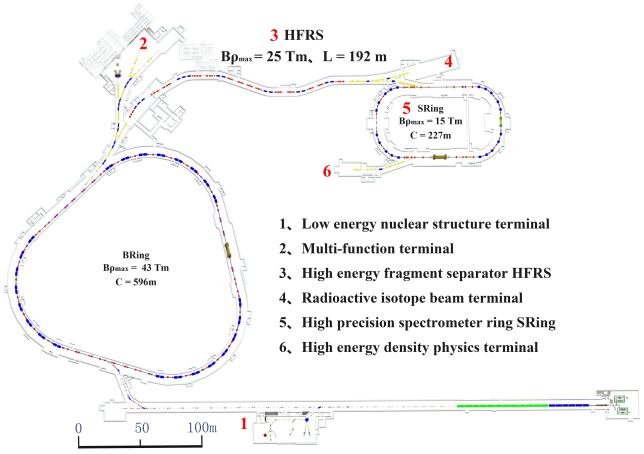

Fig. 1. (Color online) Layout of the HIAF facility.

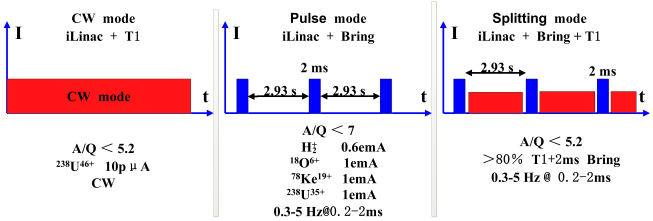

Fig. 2. (Color online) iLinac operation mode and beam parameters.

wave resonator (HWR) SRF cavities operating at a frequency of 162.5 MHz. The DBPPM electronics operates at frequencies of 81.25 MHz and 162.5 MHz. Considering the headroom required for beam steering and current variations, the electronic devices must have a dynamic range of 55 dB [4]. This dynamic range is extended to 65 dB to meet the beam measurement requirements of other linac machines built at our institute, such as the cancer therapy machine and Proton Radiation Effects Facility (PREF), with a maximum current of up to 5 mA. For position measurements, the objective is to achieve a resolution of $< 1\%$ of the half-aperture, equating to 0.2 mm in this instance. The phase resolution must be 0.15° with an absolute precision of 0.5°. The requirements for the iLinac DBPPM system are summarized in Table 1 For a high-intensity, CW superconducting iLinac, beams that are not properly steered or present insufficient quality may potentially damage or destroy accelerator components. Small beam losses can cause major problems in close proximity to the SRF accelerating structures. As a rule of thumb, the maximum beam loss along the SRF iLinac should not exceed the equivalent of 1 W/m [5]. The fast protection systems of the iLinac are mandated to detect and remove the beam within 20 μs. This imposes several critical requirements on the DBPPM system, which serves as a key input to the machine protection system (MPS). The electronic processing time for the beam position and phase calculation is approximately 3.5 μs, as described in reference [6], thereby ensuring a prompt response time for the fast interlock output when the beam position or phase deviates beyond the set threshold values [7]. In addition, because the number of BPMs is more abundant at the iLinac than at the ACCTs and DCCTs, the sum signals are calibrated to capture the beam loss in the beam intensity.

Internal research and development of DBPPM electronics began in 2018. The following sections demonstrate that the performance concerning critical specifications have not only been met but even exceeded.

Table 1. Requirements of iLinac DBPPM electronics.

Parameter	Value
Dynamic range	−65 dBm to 0 dBm
Position resolution	< 0.2 mm
Phase resolution	< 0.2°
Fast interlock response time	<5 μs
Bandwidth	Wide band: 1 MHz (data rate: 5 Msps) Narrowband: 0.2 MHz (data rate: 1 Msps)
Operation mode	CW, pulsed
Other functions	Self-calibration, Self-test

II. DBPPM SYSTEM ARCHITECTURE

The hardware architecture of the DBPPM system, which consists of an analog front-end (AFE) and a motherboard, is shown in Figure 3. The system was constructed in a modular manner, adhering to industrial standards. After signal filtering, amplification, and sampling by the analog-to-digital converter (ADC) on the AFE, the digital data are transferred to the motherboard through the fully populated high-pin count field programmable gate array (FPGA) mezzanine-connector (FMC) slots. The motherboard employs a high-performance ZYNQ UltraScale+ Multi-Processing System on Chip (MPSoC) chip XCZ9EG from XILINX, which is characterized by a high number of system logic cells and digital signal processing (DSP) slices. It features two FMC slots for hosting up to two BPMs. Differentiation of the sum signals representing the beam intensity with adjacent DBPPMs can be realized by data communication through multi-gigabit links (SFP+ interface). The electronics realizes under-sampling to convert the first/second harmonic of the beam radio frequency (RF) signal to an intermediate frequency (IF). The I/Q demodulation technique is then employed for beam position and phase measurements at various configurable data rates/bandwidths, following down-mixing, low-pass filtering, and decimation [8].

The structure graph of the AFE of the DBPPM system is shown in Figure 4 [9]. Each signal channel incorporates two low-noise amplifiers with a noise figure of 1 dB and a digital step attenuator. This attenuator offers a dynamic range of 31 dB with a resolution of 0.25 dB [10]. Following the filters, amplifiers, attenuators, and matching circuits on the AFE, the amplitude of the analog output signal is optimized to fall within the ideal input range of the ADCs for sampling. The system includes the LTC2208 ADC chip, characterized

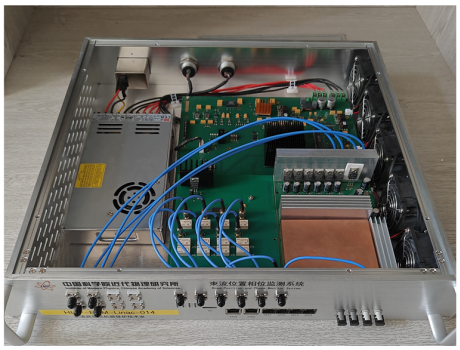

Fig. 3. (Color online) Basic hardware architecture of the DBPPM system.

by its 16-bit resolution and a maximum sampling rate of up to 130 Msps. Each receiver also incorporates a low-pass filter with a cut-off frequency of 500 MHz that can be applied to different beam bunching frequencies ranging from 1 MHz to 500 MHz. The AFE houses six RF channels: four are designated for the RF BPM signals, one is allocated for the calibration signal, and the other is reserved for the RF reference signal to perform IQ demodulation [11, 12]. The RF reference signal is obtained from a low-level RF (LLRF) system that is phase-locked with the beam. All the BPM signals along with the RF reference signal are directly under-sampled to the digital IF data streams with no analog down-conversion circuits involved.

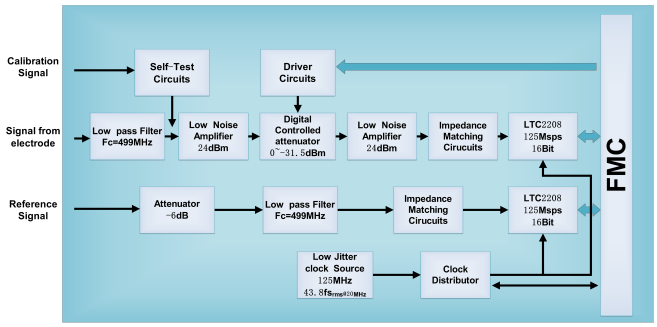

Fig. 4. (Color online) Structured graph of the AFE of the DBPPM.

Extensive attention has been given to the design of the AFE to ensure maximum dynamic range, high reliability and stability, low noise performance, and precise self-calibration. To minimize the system noise and obtain a high measurement resolution, the ADC and front-end circuit are powered by a low-noise linear power supply (TPS7A47), which features an ultra-low output voltage noise of 4 μVrms [13]. Another key element in the RF front-end signal chain is the amplifier, which significantly affects the final signal-to-noise ratio (SNR). TQP3M9019 is implemented using a low-noise figure of 1 dB. In addition, for high-speed ADCs, clock jitter is another factor that causes SNR loss. Digitizing high-speed signals to a high resolution requires careful selection of a clock that does not compromise the sampling performance of the ADC. The crystal oscillator CVHD-950-125.00 was chosen because of its low phase noise and clock jitter of 43.8 fs @122.88 MHz [14]. The clock distributor gives rise to another jitter of 61 fs @122.25 MHz [15]. Thus, the total jitter of the entire sampling system is [16, 17]

$$T_{\text{jitter}} = \sqrt{(43.8)^2 + (61)^2} = 75.1\,\text{fs}$$

The theoretical limit of the SNR resulting from clock jitter is given by

$$SNR = 20\log_{10}(2\pi * f_{\text{in}} * T_{\text{jitter}}) = 82.38\,\text{dB}$$

where f_{in} is the input frequency 162.5 MHz. Consequently, the clock effective number of bits (ENOB) is decreased to [18, 19]

$$ENOB = (\text{SINR} - 1.76)/6.02 = 13.38\,\text{bits}$$

,

where SINR denotes the signal-to-noise and distortion ratio. Therefore, the number of significant bits is guaranteed to be 13.38 bits at a sampling rate of 125 MHz.

To further maintain the electronic performance, the characteristic impedance of the analog signal transmission line from the input of the AFE to the ADC front end is matched to 50 Ω to avoid signal reflection and overlap, which can result in position and phase measurement errors. For the digital part, the deviation of characteristic impedance is controlled within ±5% for both single-ended signaling with 50 Ω and differential signaling with 100 Ω. The sampling clocks of the five ADCs are of the same length. To maintain a wide dynamic range with low noise in hostile digital environments, the entire AFE comprises six layers based on high-speed circuit design techniques, including proper signal routing, decoupling, and rounding. Low-impedance large-area ground planes are implemented to obtain good isolation between the signal layers and between the signal and power layers. The analog and digital circuits are well isolated using ferrite beads. The ground plane not only acts as a low-impedance return path for decoupling high-frequency currents (caused by fast digital logic) but also minimizes EMI/RFI emissions. Also, a copper shielding block is utilized on the AFE to achieve good immunity to the EMI. The resulting crosstalk between channels is listed in Table 2. The most significant crosstalk observed was −82 dB, occurring between channels B and D. Thus, the signal isolation between the channels of the RF circuits is good enough and the effect on position measurement is completely negligible.

Table 2. Crosstalk between the channels on a single DBPPM.

Specimen	A (dB)	B (dB)	C (dB)	D (dB)
A	/	-93	-96	-91
B	-92	/	-94	-82
C	-98	-97	/	-87
D	-89	-83	-87	/

The motherboard based on XCZ9EG mainly consists of two parts. The first part is called programmable logic (PL),

which consists of 600 K logic units, 2520 DSP slices, total RAM of 40.9 Mb, hundreds of high-performance I/Os, and multiple high-performance high-speed connectivity modules [20–22]. All digital signal processing of the beam position and phase algorithms is performed in the PL, which has a high-speed ability to process mass data and can be run in parallel in real time. The second part integrates a quad-core ARM Cortex-A53 and a dual-core ARM Cortex-R5F-based application processing system (PS) that is responsible for all communications with the control system and coordinates all on-board functionalities. A control system employing the Experimental Physics and Industrial Control System (EPICS) has been developed. Each DBPPM electronic device incorporates an Ethernet-based embedded input-output controller (IOC) for data processing and interfaces with the EPICS control system through TCP/IP. The board is equipped with a 16 GB SO-DIMM DDR4 memory module, providing program memory space for the PS and a large circular buffer for postm-ortem (PM) data storage in the event of an MPS trigger. This buffer, with a depth of 2 GB, can store the position, phase, and amplitude data for each channel at a rate of 1 Msps, covering the last 2 s prior to the MPS trigger and the time interval thereafter. The maximum throughput of the memory is 21.3 GB/s, which is sufficient for storing continuous bursts of raw ADC data and offering programming and data memory for the PS. The motherboard includes a 4 GB embedded multimedia card (eMMC) nonvolatile memory, FPGA bitstream storage, and PS program data. Upon powering, the FPGA configures itself from the eMMC memory. When the PS finishes reset, it runs a small boot loader program using its internal memory. This boot loader fetches the final program from the eMMC and copies it to the DDR memory, from which it is executed.

III. DBPPM PERFORMANCE TEST IN LABORATORY

To evaluate the performance of this electronic system, a series of focused tests was conducted under laboratory conditions, including noise measurement, long-term drift with respect to temperature changes, accuracy, and resolution of the position and phase measurements.

A. Electronic noise measurement

DBPPM electronics will be used for low-intensity beams with beam currents down to 10 μA at the machine commissioning stage, especially for ions that are difficult to produce in the ion source. According to the simulations, the peak voltage of the signal induced on the BPM electrode can be as low as 100 μV. Thus, the electronic noise must be controlled at an extremely low level to obtain a better SNR for weak beams. Electronic noise can be evaluated by measuring the distribution width of the raw data when all RF inputs are open. Figure 5 shows the statistical distribution of the raw ADC data with 10 k points for the four RF signal channels and one reference signal channel. The fitting variance of the noise distribution is below 9, which is small enough compared to the dynamic range from +32767 to -32767 in the 16-bit ADC LTC2208. These results indicate very good background noise control of the electronics as a whole. In addition, the measured data show slightly different offsets between the different channels, which can be easily corrected in subsequent signal processing.

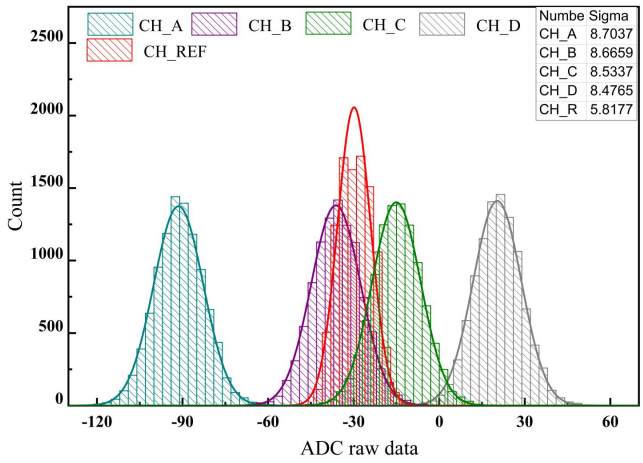

Fig. 5. (Color online) Fitting analysis of noise distribution for different channels in DBPPM.

B. Phase and position resolution measurement results

A signal generator was used to simulate the beam-induced and reference signals using power splitters. The RMS values of the phase and position were measured by varying the input power of the RF signal from −65 dBm to −10 dBm. For each input power, 10 k points were collected and statistically analyzed at a data rate of 1 Msp and DBPPM geometric factor of k = 10 mm. Figure 6 shows the variance in the position and phase values as a function of the input signal levels. Note that the resolution improves with increasing signal levels, as expected. When the input signal power is above −30 dBm, the RMS values are stable because the attenuators on the AFE are adjusted to avoid electronic saturation, and the equivalent power no longer increases. According to the measurement results, for input power levels exceeding −45 dBm, position resolutions of 4 μm and phase resolution of 0.04° are achieved, which correspond to normal operation signal level, correlating with a beam current of more than 100 μA at the iLinac. For the low-current beam down to 10 μA, the beam-induced signal amplitude is close to −65 dBm [4]. In this case, the position resolution is 33 μm, and the phase resolution is approximately 0.16°. All these values constitute better performance than the prescribed measurement requirements.

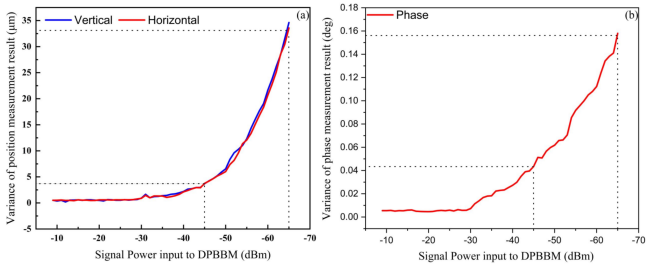

Fig. 6. (Color online) Variance of position and phase measurement results vs input power.

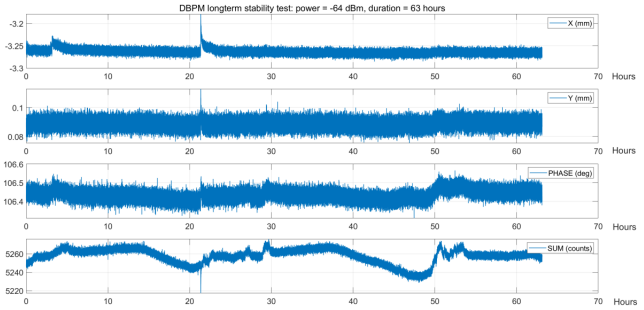

Fig. 7. (Color online) Long-term stability measurement for position and phase during 63 hours with temperature changes of approximately 10 °C.

C. Long-term drift measurement results

Beam phase measurement on iLinac is critical for machine tuning, optimal beam acceleration, and troubleshooting. To determine the nominal RF settings for matching bunches with respect to the phases of various cavities, the phase measurement must be accurate and reliable, and ensure good stabilization characteristics with respect to temperature changes. Long-term drifts in the position, phase, and sum signals are shown in Figure 7. The sudden large change was accidentally caused by a connecting cable inadvertently moved during the test. During the 63-hour measurement with input signals of 0.5 h at full-scale dynamic range of the ADC, the environmental temperature changed by approximately 10 °C. The test began at 8 am. Then, the temperature was gradually increased from 6 o'clock in the morning to 21 o'clock at night. It decreased dramatically from 21 o'clock at night to 6 o'clock in the second morning. We can clearly see that the sum signal and phase measurement results exhibit a changing trend according to the 24-hour cycle. The sum increased with increasing temperature and decreased with decreasing temperature. The reason for the sum-signal variation is that the gains of the amplifiers are more sensitive to temperature changes. The reasons for the phase change are complicated and may be due to the change in the cable length caused by temperature changes and electronic drift. However, the total change in phase was less than 0.05° after 63 hours, so it should be ignored. Meanwhile, the DBPPM position was varied only by 10 μm over the whole 63-hour trial, which indicates that the DBPPM channels were consistent, and the same drift errors cancelled each other out when performing the position calculation. Nevertheless, this small long-term drift can be deemed negligible, and it can be concluded that the developed DBPPM electronics is stable enough.

D. Self-test and self-calibration function

At the iLinac, the cables connecting the BPMs [4, 23] in the tunnel to their corresponding DBPPM electronics outside the tunnel will reach 100 m. These long RF cables vary from BPM to BPM and are exposed to uncontrolled temperature environments. This environmental impact on the BPM cable propagation parameters may cause long-term drifts in the measured beam phase. To ensure accurate phase measurements, it is necessary to measure and compensate for the differences in RF cables between BPMs, as well as the phase shift caused by environmental changes in cables and electronics. However, verifying and measuring these parameters after the installation of BPMs, cables, and DBPPM electronics is challenging and time-consuming, particularly when accuracy checks of phase measurements are required during machine commissioning. This calls for the exploration of self-test and self-calibration functions, as illustrated in Figure 8. The calibration signal originates from the LLRF system and is phase-locked to the beam, similar to the reference signal, at a level of approximately 15 dBm. Through a carefully designed splitter and high-precision isometric delay for each channel, this calibration signal can be routed to each RF signal channel with an attenuation of 20 dB or to individual BPM electrodes. When directed to the electronics, it enables the measurement and correction of the channel-to-channel gain and group delay differences as well as the position and phase offset for each DBPPM. Consequently, the calibration of the electronics can be executed swiftly and automatically in a laboratory using appropriate software controls and calculations. To assess RF cable differences, the calibration signal can be transmitted to one electrode with the coupled signal measured from adjacent electrodes. For instance, when the calibration signal is sent to electrode A of the BPM, the phase of the coupled signal from electrodes B and D can be characterized as follows:

$$\varphi_{\mathrm{A\,B}} = \omega\,(t_{\mathrm{A}} + t_{\mathrm{B}}) + \varphi_{\mathrm{B\,E}}$$

$$\varphi_{\mathrm{A\,D}} = \omega\,(t_{\mathrm{A}} + t_{\mathrm{D}}) + \varphi_{\mathrm{D\,E}}$$

where ω is the signal-processing frequency, t_{A} is the RF cable delay from electrode A to the electronics, and $\varphi_{\mathrm{B\,E}}$ is the phase of the reference signal relative to the calibration signal through channel B inside the DBPPM electronics, as in channel D. In this context, the differences in the electromagnetic field transmission time between the electrodes are disregarded under the assumption that mechanical accuracy can ensure their insignificance. Because phases $\varphi_{\mathrm{B\,E}}$ and $\varphi_{\mathrm{D\,E}}$ can be measured and corrected in advance or at any time if needed, the cable difference between B and D can be obtained. Similarly, the cable differences between different BPMs units can

be measured and corrected remotely. Additionally, the device can be used for self-testing whenever the electronic devices are restarted or must be checked. The signal path from the BPM electrode to the electronics can be checked by measuring the coupled calibration signal fed in the other BPM electrodes, and the electronics itself can be implemented with a calibration signal entering the electronics and cables to the BPM sensors disconnected. If the measured amplitudes for each channel in each condition fall out of the set thresholds, the fault status is reported to the operator and MPS. This calibration tool can be applied to diagnose and locate internal faults accurately and conveniently if something is incorrect in the BPM system.

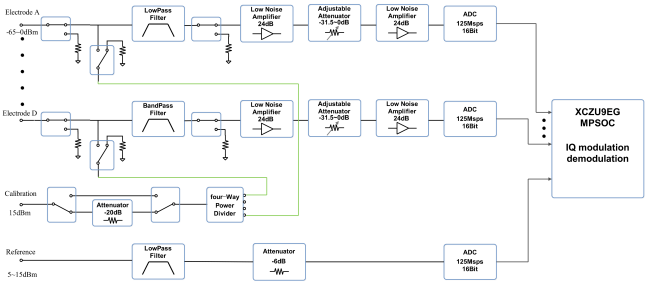

Fig. 8. (Color online) Structured graph of the calibration and self-test circuits of the DBPPM.

To verify the performance of on-line measurement and compensation for the differences in RF cables, a lab test was performed, as depicted in Figure 9. The calibration signal was transmitted to electrode A of a button BPM, and the coupled signal from electrode B was measured. Six short cables with a length of 217 mm were added to signal transmission path B one at a time. The measured phase values and their distribution for every insertion are shown in Figure 10, where the phase is shifted by 51.8°. The phase shift was also measured using a network analyzer for different cable lengths, as shown in Figure 11. The results at a frequency of 162.5 MHz are compared in Figure 12 and agree well. The Pearson product-moment correlation coefficient (PPMCC) is as high as 0.9999 and the deviation is within ±0.06°, which is accurate enough for compensation of the differences in RF cables.

E. Real-time 2D non-linear corrections on FPGA

At the iLinac, button BPMs are assembled inside the cryomodules, and capacitance BPMs are mounted in normal temperature regions [24–26]. Four electrodes are installed orthogonally for each BPM. With the traditional linear approach of the difference-over-sum method, both types have limited linear regions for accurate beam position measurement. Moreover, this method cannot satisfy the iLinac requirement of position threshold settings for the beam interlock function. General real-time linearization methods are based on linear correction combined with a simplistic polynomial, which may lead to inaccuracies in their limited applications. Only 2D non-linear polynomial correction [27–29]

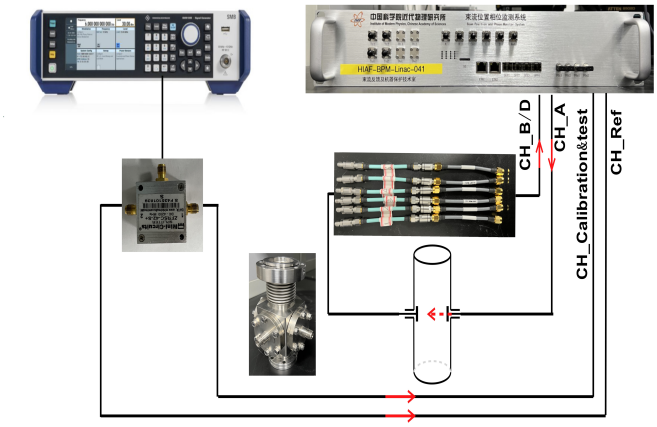

Fig. 9. (Color online) Lab test setup for phase verification of measurement and compensation with different RF cables.

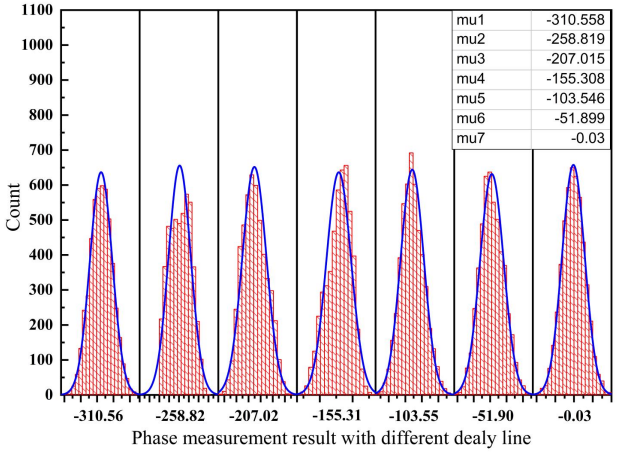

Fig. 10. (Color online) Phase distribution measurement (5000 points) for each cable inserted (from left to right, with insertion of 0 to 6 cables).

can suppress the non-linear effects of button BPMs by considering the cross-coupling between XY planes.

$$x_{\mathrm{bpm}}^{2D} = \sum_{i,j=0}^{p,q} \left(c_{ij} x_{\mathrm{raw}}^{i} \, y_{\mathrm{raw}}^{j} \right)$$

$$y_{\mathrm{bpm}}^{2D} = \sum_{i,j=0}^{p,q} \left(c_{ij} y_{\mathrm{raw}}^{i} \, x_{\mathrm{raw}}^{j} \right)$$

Here, C_{ij} is a set of calculated coefficients for each corresponding plane X and Y, x_{raw} , y_{raw} are difference-over-sum values from BPM signals, and p and q are maximum powers of each variable. This 2D correction has been used, for instance, in CERN. However, the data are mainly analyzed off-line. For real-time measurement and fast machine protection interlock, all corrections must be realized on an FPGA, which is included in the DBPPM electronics. For brevity, and

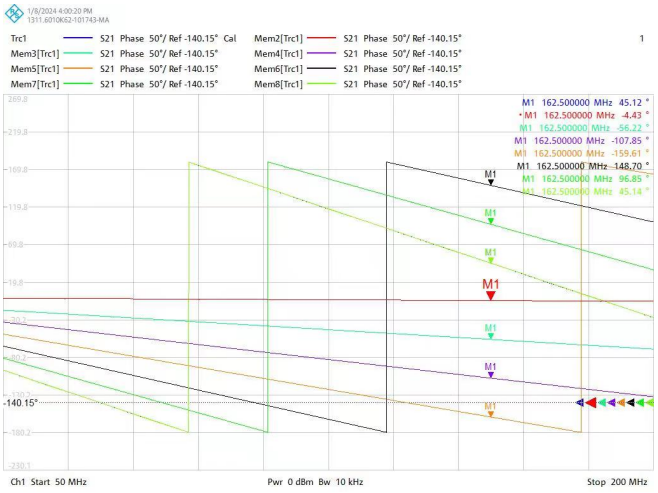

Fig. 11. (Color online) Phase shift measurement with a network analyzer (from up to down, with 0 to 6 cables inserted in the transmission).

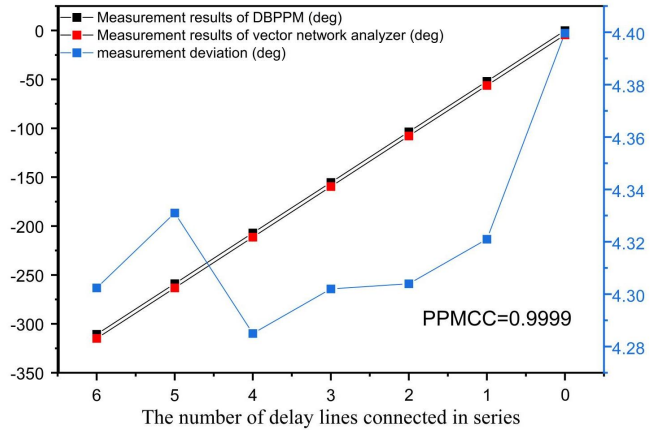

Fig. 12. (Color online) Comparison of phase measurement between a DBPPM and a network analyzer; both results agree well and the deviation is within $\pm 0.06°$. The horizontal axis represents how many cables are inserted.

considering the FPGA computing resources available, only 4th–order polynomials were realized. Figure 13 compares the mapping results with and without 2D non-linear polynomial correction for a button BPM with an aperture of $40\,\mathrm{mm}$; the value of k is 10.7. A stretched metal wire moved by servomotors and controlled by a PL controller can accurately obtain position information with a resolution of only a few µm. According to the mapping results, low-power polynomials provide sufficient quality correction. Even with a large offset of $10\,\mathrm{mm}$, DBPPM can obtain accurate position measurements with an error of less than $100\,\mu\mathrm{m}$, as shown in Figure 14 [30].

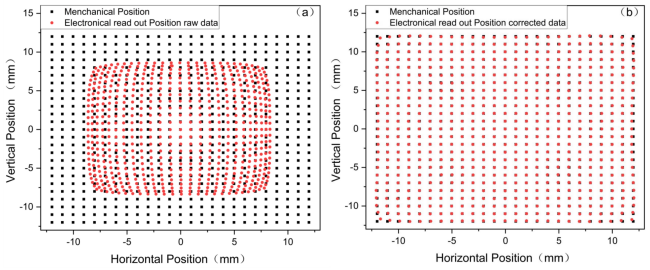

Fig. 13. (Color online) Mapping results without (a) and with (b) 2D non-linear polynomial correction; red dots: wire position measured by DBPPM, black dots: wire position from PL controller.

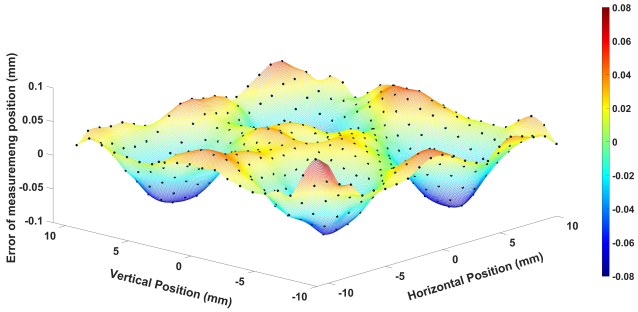

Fig. 14. (Color online) Error analysis after 2D non-linear polynomial correction.

IV. SOFTWARE INTEGRATION

Figure 15 depicts the software integration architecture. After IQ demodulation and decimation of the PL, the amplitude of each channel, position, phase, as well as the sum signal at both processing frequencies are acquired at data rates of either $5\,\mathrm{Msps}$ or $1\,\mathrm{Msps}$. To facilitate real-time data transmission from the PL to the PS, a memory-mapped-based AXI4 interface featuring a dual BRAM setup is employed to avoid conflicts in writing and reading [31]. This configuration can achieve a transmission rate of up to $118\,\mathrm{MB/s}$. The BRAM controller was designed to interconnect with the AXI and integrate it with the system master for communication with the local block RAM. It supports both single and burst transmissions to block RAM, and its performance has been optimized. To transmit and view raw data or decimated raw data, either in triggered mode or with a configurable refresh frequency, the same interface is utilized but with a singular BRAM. The lighter version of the AXI protocol, AXI4-Lite, is a simpler protocol suited for less demanding interfaces and is typically used for register-style control/status interfaces [32]. Therefore, it was implemented for data transmission of the state machine, interlock signal, and command and state transmission of the self-test and self-calibration modules. A control system based on EPICS was developed to configure the environment of the distributed control system. The DBPPM electronics utilizes Ethernet-based embedded IOC for data processing, saving, viewing, and communicating with EPICS via TCP/IP.

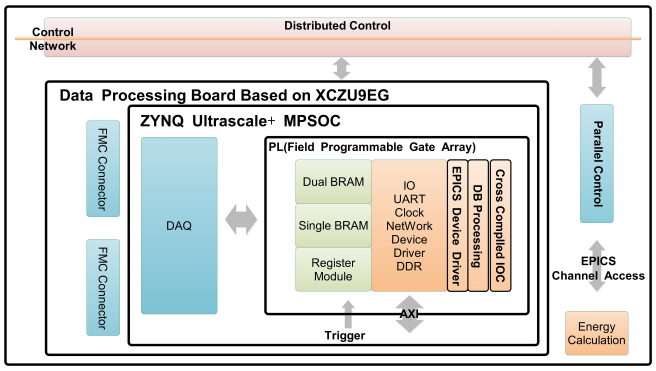

Fig. 15. (Color online) Software integration architecture.

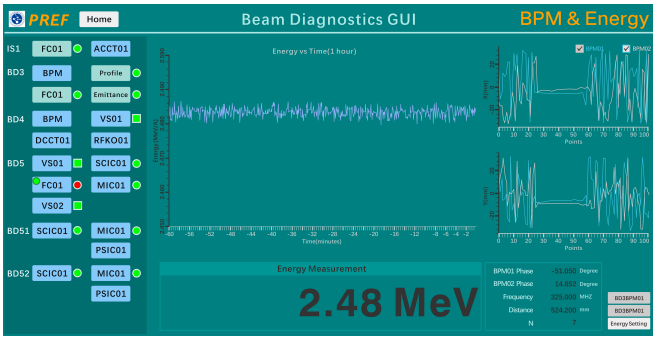

Fig. 16. (Color online) Screenshot of on-line beam position, phase, and energy measurements on PREF.

V. BEAM MEASUREMENT RESULTS

Although the DBPPM electronics was originally developed for the HIAF project, 17 units have already been installed and operated on several linac machines for beam position and phase measurement, such as the Heavy-Ion Research Facility in Lanzhou (HIRFL) [33], Proton Radiation Effects Facility (PREF), and Chinese Accelerator Facility for Super-heavy Elements [34] (CAFE). Here, the beam measurement results with DBPPM electronics on the PREF linac are described as an example. The PREF machine, which was built and commissioned by our institute in August 2023, consists of a linac as its injector, a synchrotron for further acceleration, and two extraction lines for the radiation experiment. The pulsed proton beams, with a pulse length of 40 μs and current of approximately 2.5 mA, were accelerated to 2.48 MeV by an RFQ with an RF frequency of 325 MHz. To obtain proper settings of the RFQ and match the injection of the synchrotron, accurate energy measurements are critical. They are performed by two BPMs installed after the RFQ. The beam velocity can be determined by the time of flight between two BPMs, that is, two measured phase differences [35]:

$$V_{\mathrm{p}} = \frac{L}{\frac{1}{f_{\mathrm{RF}}} \times \left(N + \frac{\varphi_{\mathrm{BPM1}} - \varphi_{\mathrm{BPM2}} + \Delta\varphi_{\mathrm{corr}}}{2\pi} \right)}$$

where L=524.2 mm is the distance between two BPMs, fRF=325 MHz is the signal processing frequency, N=7 is the integer RF period between the two BPMs, and $\Delta\varphi_{\mathrm{corr}}$ is the phase correction owing to the cable length difference. The energy is expressed as

$$E = 938.272\mathrm{MeV/u} \times \left(\frac{1}{\sqrt{1 - \left(\frac{v_{\mathrm{p}}}{\mathrm{c}}\right)^2}} - 1 \right)$$

where c is the speed of light [36, 37].

Figure 16 shows a screenshot showing on-line beam measurement results of two BPMs. The main image in the middle shows the average energy per pulse for 1 hour. The two figures on the right show the horizontal and vertical position results for one macro-pulse with a plus length of 10 μs. Figure 17 shows the historical data for the average position and energy per pulse over 1 week. According to the statistical distribution of the long-term measurement data, from pulse to pulse, the position variance was 0.54 mm and the energy variance was 0.001 45 MeV, which is reasonable. By comparing the energy measured by DBPPM and the cavity voltage from

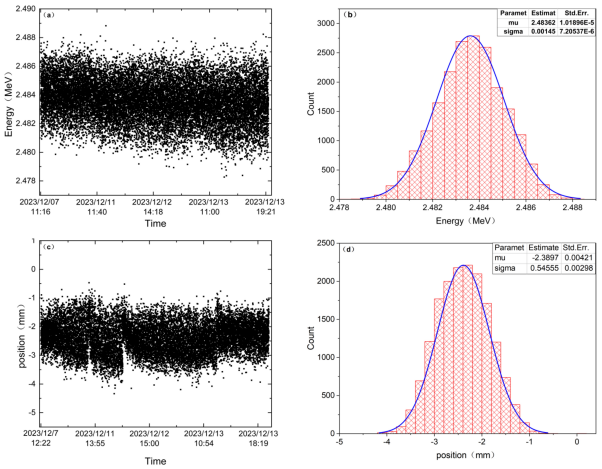

Fig. 17. (Color online) BPM energy and phase measurement results, and related statistical distribution over one week.

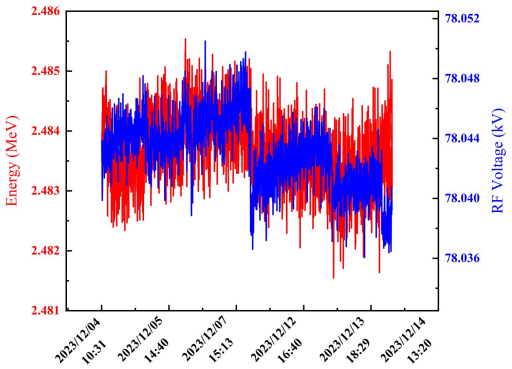

Fig. 18. (Color online) Long-term monitoring of beam energy and RFQ cavity voltage of PREF.

an RFQ cavity pickup, a very good correlation is observed in Figure 18. Small changes in the cavity voltage resulted in a corresponding drift in the beam energy. According to long-term on-line operation, it can be concluded that the DBPPM electronics is reliable and stable, and the measurement is accurate and reasonable. DBPPM systems are frequently used in machine studies, diagnostics, and troubleshooting.

VI. SUMMARY

HIAF iLinac DBPPM electronics based on the ZYNQ UltraScale+ MPSoC was developed and operated for beam measurements on other linac machines. Through a meticulously engineered analog front-end and superior algorithms, the proposed DBPPM is capable of attaining a wide dynamic range of $65\,\mathrm{dB}$, along with exceptional position and phase resolution. The concept of self-calibration performs well and provides online measurements of position and phase offset, as well as the internal fault diagnosis of the DBPPM system. With 2D non-linear polynomial correction implemented on an FPGA, even with a large offset of $10\,\mathrm{mm}$ for button BPMs, the DBPPM can obtain accurate real-time position measurement, which is needed for the fast MPS of modern high-power machines. Both laboratory and beam measurements indicate that the electronics exhibits high performance, good long-term stability, very low noise, and a large dynamic range. All performance metrics of the system fully meet and even exceed the design requirements. Presently, all iLinac DBPPM electronic devices are being tested in the laboratory. In the middle of this year, they will be installed on-line for long-term stability tests and preparation for machine commissioning.

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